# APOSTOLOS DOLLAS

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## EDUCATION

University of Illinois at Urbana-Champaign: Ph.D., Computer Science, 1987.
University of Illinois at Urbana-Champaign: MS, Computer Science, 1984.
University of Illinois at Urbana-Champaign: BS, Computer Science, 1982.

## PROFESSIONAL EXPERIENCE

Technical University of Crete (December 1993 – present): Professor of ECE, Director, Microprocessor and Hardware Lab (1994 – present), Associate Professor (December 1993 – May 2001), Chairman (1995-1997), Associate Chairman (1997-2001). University Senate-appointed Director of campus-wide computer network project (1999-2002, 1995-1997). Member of University Senate (several terms). Undergraduate courses on Logic Design, Digital Processors, Computer Organization, Computer Architecture, VLSI/ASIC Design. Perform research and teach graduate courses on reconfigurable computing, computer architecture, rapid system prototyping, application specific processor design, and computer hardware.

Member of the Computer Architecture and VLSI Systems Division (CARV), Institute of Computer Science, Foundation of Research and Technology, Hellas (ICS- FORTH), (1994-present). Participation in the second generation architecture and first generation implementation of the *Telegraphos* high speed computer networks project (1994-1995).

Duke University, N. Carolina, USA (1986-1994) Assistant Professor of ECE, secondary appointment as Assistant Professor of CS. Undergraduate and graduate courses on digital systems implementation, logic design, computer architecture, microprocessors, VLSI design. Research on computer architecture, rapid system prototyping, hardware and software tools for high performance systems, VLSI testing.

Consultant to companies and universities (1988-1994) including the University of North Carolina (Chapel Hill), Microelectronics Center of North Carolina (MCNC), Industrial Innovators, Inc., on subjects which include system and circuit design for high resolution imaging by modifying CAT scan equipment, reverse engineering issues for cotton processing equipment, and computer architecture/VLSI systems design and test.

University of Illinois at Urbana-Champaign (UIUC), (1982-1986): Teaching Assistant in undergraduate and graduate courses on computer hardware, Research Assistant (summers of 1983,1985) on siftware engineering projects funded by NASA and IBM. Graduate researcher and chief architect of the UNIFIELD computer, a 64-node SIMD architecture with unary representation. Graduate researcher on analog signal transmission through optical fibers.

Institute of Solid State Physics and Lasers, Foundation of Research and Technology, Hellas (FORTH): Graduate researcher (summer, 1984), software and hardware for the implementation of Greek character sets.

## PUBLICATIONS

### A. Fully Refereed Journals

1. G. Chrysos, A. Dollas, N. Bourbakis, Architecture and Design of an Embeddable System for SCAN-Based Compression, Encryption and Information Hiding, *Journal of Real Time Image Processing,* Special Issue on Field Programmable Technology, Springer, vol. 2, no. 4, pp. 207-222, December, 2007.
2. E. Sotiriades, A. Dollas, "A General Reconfigurable Architecture for the BLAST algorithm", *The Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology,* Special Issue on Computing Architectures and Acceleration for Bioinformatics Algorithms, Kluwer Academic Publishers, Vol. 48 , No. 3, pp.189 - 208, September, 2007.
3. K. Papademetriou, S. Sotiropoulos, A. Dollas, Low Cost Real-Time 2D Motion Detection based on Reconfigurable Computing, *IEEE Transactions on Instrumentation and Measurement,* vol. 55, No. 6, pp. 2234-2243, December, 2006.
4. E. Koutroulis, A. Dollas, K. Kalaitzakis, "High Frequency Pulse Width Modulation Implementation using FPGA and CPLD ICs", *Journal of Systems Architecture,* Elsevier Press, vol. 52, No. 6, pp. 332-344, June 2006.
5. A. Dollas, S. Sotiropoulos, K. Papademetriou, A 2D Motion Detection Model for Low Cost Embedded Reconfigurable I/O Devices, *IEEE Transactions on Biomedical Enginering*, vol. 52, No. 8, pp. 1443-1449, August, 2005.
6. C. Kachris, N. Bourbakis, A. Dollas, A Reconfigurable Logic Based Processor for the SCAN Image and Video Encryption Algorithm, *International Journal of Parallel Programming*, Kluwer Academic Publishers, Vol. 31, No. 6, pp. 487-504, December 2003 (extended version of the WASP 2002 paper with additional results).
7. N. Bourbakis, A. Dollas, SCAN Based Video Compression-Encryption-Hiding for Multimedia on Demand*, IEEE Multimedia*, pp. 79-87, July-September, 2003.
8. P. Stogiannos, A. Dollas, V. Digalakis, A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition using Hidden Markov Models, *Journal of VLSI Signal Processing*, Kluwer Academic Publishers, vol. 24/(2/3), pp.223-240, March, 2000.
9. A. Dollas, W. Rankin, D. McCracken, New Algorithms for Golomb Ruler Evaluation and the Proof of the 19-Mark Ruler, *IEEE Transactions on Information Theory,* vol. 44, no. 1, pp. 379-382, January 1998.
10. M. Katevenis, E. Markatos, G. Kalokerinos, A. Dollas, Telegraphos: A Substrate for High Performance Computing on Workstation Clusters, *Journal of Parallel and Distributed Computing*, vol. 43, No. 2 pp. 94-108 Academic Press, June, 1997.

11. K.Boland, A. Dollas, Predicting and Precluding Problems with Memory Latency, *IEEE Micro*, Vol. 14, No. 4, pp. 59-67, August , 1994.
12. M.P.Thint, P.P. Wang, A. Dollas, Nonparametric Graded Data Processing with Back-Error Propagation Networks, *Information Sciences*, Vol. 67, No.1/2, pp. 167-188, Elsevier Science Publishing Co., January , 1993.
13. R.F.Krick, A. Dollas, The Evolution of Instruction Sequencing, *IEEE Computer*, Vol. 24, No. 4, pp. 5-15, April, 1991.
14. D.J. Wagenaar, F.A. DiBianca, C.R.Tenney, J.E.Vance, M.S.C.Reed, D.W.Wilson, A. Dollas, D.L.McDaniel, P.Granfors and S.Petrick, A Computer Controlled X-Ray Imaging Scanner Using a Kinestatic Charge Detector, *Review of Scientific Instruments*, Vol. 61, No. 2, pp. 701-711, February, 1990.

**B. Books**

1. The Art of Microelectronic Systems, A. and K. Peters Publishers, Ltd., (in preparation).

**C. Book Chapters**

1. A. Dollas, J.D.S. Babcock, Rapid Prototyping of Microelectronic Systems, Advances in Computers, M.V.Zelkowitz (Ed.), Vol. 40, pp. 66-125, Academic Press, New York, 1995.
2. A. Dollas, G. Gastrodale, A. Knowledge Based Enviroment for Integrated Circuit Testing, Artificial Intelligence Methods and Applications, N. Bourbakis, (Ed.), Vol. 1, pp. 637-674, World Scientific Press, 1992.
3. W.J. Poppelbaum, A. Dollas, J. Glickman and C.O'Toole, Unary Processing, Advances in Computers, M. Yovitts (Ed.), Vol. 26, pp. 47-92, Academic Press, New York , 1987.

**D. Editorial Work**

1. A. Dollas, N. Kanopoulos, guest editors, Special Issue on Rapid System Prototyping of Microelectronic Systems, IEEE Computer, February, 1995, Computer Society Press.
2. Member of the Editorial Board, International Journal of Artificial Intelligence Tools, World Scientific Press, 1990-1993.
3. Proceedings, The Second International Conference on Tools for Artificial Intelligence, A. Dollas, W.T. Tsai and N. Bourbakis, editors, Computer Society Press, 1990.

**E. Full Conference Papers, Fully Refereed**

1. E. Sotiriadis, C. Kozanitis, G. Chrysos, A. Dollas, Rapid Prototyping of a System-on-a-Chip for the BLAST Algorithm Implementation, Proceedings, 17th International IEEE Workshop on Rapid System Prototyping, (RSP), pp.223-229 , Chania, Greece, June 16-18, 2006, Computer Society Press.
2. E. Sotiriadis, C. Kozanitis, A. Dollas, FPGA Based Architecture for DNA Sequence Comparison and Database Search, Proceedings, 13th Reconfigurable Architectures Workshop (RAW), April 25-26, Rhodes, Greece, 2006 (on-line proceedings under the IPDPS conference).
3. E. Sotiriadis, C. Kozanitis, A. Dollas, Some Initial Results on Hardware BLAST Acceleration with a Reconfigurable Architecture, Proceedings, 8th Workshop on High Performance Computational Biology (HiCOMB), April 25, Rhodes, Greece, 2006 (on-line proceedings under the IPDPS conference).
4. A. Dollas, K. Papademetriou, E. Sotiriades, *et al.*, , "A Case Study on Rapid Prototyping of Hardware Systems: the Effect of CAD Tool Capabilities, Design Flows, and Design Styles", in Proceedings, 15th International IEEE Workshop on Rapid System Prototyping RSP-2004, June 28-30, 2004, Geneva, Switzerland, Computer Society Press.

5. A. Dollas, D. Efstathiou, T. Kyriakides, "A Universal Low Cost Run-Time and Programming Environment for Reconfigurable Computing", in Proceedings, 14th International IEEE Workshop on Rapid System Prototyping RSP-2003, June 9-11, 2003, San Diego, CA, Computer Society Press.
6. A. Dollas, C. Kachris, N. Bourbakis, "Performance Analysis of Fixed, Reconfigurable, and Custom Architectures for the SCAN Image and Video Encryption Algorithm", in Proceedings, 11th International IEEE Symposium on Field-Programmable Custom Computing Machines, Napa Valley, April 9-11, 2003, Computer Society Press.
7. C. Kachris, S. Manniccam, A.Dollas, N. Bourbakis, A Reconfigurable Logic-Based Processor for the SCAN Image and Video Encryption Algorithm, 1st Workshop on Application Specific Processors (WASP1), Istanbul, Turkey, November 19, 2002.
8. A. Dollas, D. Pnevmatikatos, N. Aslanides, *et al*., Experimental Testing of PLATO, a Reconfigurable Active ATM Network Node, Proceedings, 8th Panhellenic Informatics Conference, pp. 11-17, Nicosia, Cyprus, November, 2001 (in English).
9. A. Dollas, K. Papademetriou, N. Aslanides, T. Kean, A Reconfigurable Embedded Input Device for Kinetically Challenged Persons, Proceedings, pp.326-335, FPL 2001, Belfast, N. Ireland, August 27-29, 2001, Springer-Verlag.
10. A. Dollas, D. Pnevmatikatos, N. Aslanides, *et al*., Rapid Prototyping of a Reusable 4x4 Active ATM Switch Core with the PCI Pamette, Proceedings, 12th International IEEE Workshop on Rapid System Prototyping RSP-2001, pp. 17-23, June 25-27, 2001, Monterey, CA, Computer Society Press.
11. A. Dollas, D. Pnevmatikatos, N. Aslanides, *et al*., Architecture and Applications of PLATO, a Reconfigurable Active Network Platform, Proceedings, 9th International IEEE Symposium on Field-Programmable Custom Computing Machines, Rohnert Park, CA, April 30 – May 2, 2001, Computer Society Press.
12. E. Sotiriades, A. Dollas, P. Athanas, Hardware-Software Codesign and Parallel Implementation of a Golomb Ruler Derivation Engine, Proceedings, 8th International IEEE Symposium on Field-Programmable Custom Computing Machines, pp. 227-235, Napa Valley, April 17-19, 2000.
13. A. Dollas, E. Sotiriades, A. Emmanouelides, Architecture and Design of GE1, a FCCM for Golomb Ruler Derivation, Proceedings, 6th International IEEE Symposium on FPGA's for Custom Computing Machines, pp. 48-56, Napa Valley, April 15-17, 1998.
14. K. Tavladakis, K. Kostalias, A. Dollas, K. Kalaitzakis, N. Voulgaris, Development of a Microcontroller Based Distributed Adaptive Traffic Control System, Proceedings, 8th IFAC/IFIP/IFORS Transportation Systems Symposium, Chania, Crete, Greece, June, 1997.
15. P. Vatsolaki, G. Kalokairinos, M. Stratakis, C. Xanthaki, M. Ligerakis, G. Kornaros, A. Dollas, G. Papadourakis, M. Katevenis, The Implementation of Telegraphos: A High Speed Computer Network Architecture, 5th Panhellenic Computer Science Conference, Athens, Greece, December, 1995 (in Greek).
16. J.D.S. Babcock, A. Dollas, A Case Study of System Synthesis with Non-Synthesizable Components using Exteded VHDL, Proceedings, Sixth International IEEE Workshop on Rapid System Prototyping RSP-95, pp. 168-173, Computer Society Press, 1995.
17. A. Dollas, B. Ward, J.D. Babcock, FPGA Based Low Cost Generic Reusable Module for the Rapid Prototyping of Subsystems, Proceedings, Fourth International Workshop on Field Programmable Logic and Applications FPL-94, Lecture Notes in Computer Science, vol. 849, pp. 259-270, R.W.Hartenstein, M. Servit (Eds.), Springer -Verlag, 1994.
18. J.D.S. Babcock, A. Dollas, Extended VHDL for the Rapid Prototyping of Systems With Synthesizable and Nonsynthesizable Subsystems, Proceedings, Fifth International IEEE Workshop on Rapid System Prototyping RSP-94, pp. 146-152, Computer Society Press, 1994.

19. A. Dollas, S. Grutchfield, An Evaluation of the Teamwork CASE Enviroment for Specifications Capture of Hardware Systems, Proceedings, Third International IEEE Workshop on Rapid System Prototyping RSP-92, pp. 38-48, Computer Society Press, 1992.
20. D. Alexandrou, A. Dollas, S. Babcock, W. Karunaratne, A. System for Simultaneous Video and Acoustic Data Acquisition, Proceedings, IEEE OCEANS 92 International Conference, vol. 1, pp. 370-374, 1992.
21. D. Overhauser, A. Dollas, D. Alexandrou, A. Richardson, SeaTrace: An Interactive Modeling and Visualization Package for Sound Propagation in the Ocean, Proceedings, IEEE OCEANS 91 International Conference, pp. 465-462, 1991.
22. P.J. Christopher, A. Dollas, Knowledge-Based Process Scheduling on Symmetric Multiprocessors, Proceedings, Third International IEEE Conference on Tools for Artificial Intelligence TAI-91, pp. 493-497, Computer Society Press, 1991.
23. A. Dollas, Experimental Results in Rapid System Prototyping with Incomplete CAD Tools and Inexperienced Designers, Proceedings, Second International IEEE Workshop on Rapid System Prototyping RSP-91, pp. 9-16, Computer Society Press, 1992.
24. G.L. Castrodale, A. Dollas, D. Overhauser, V. Gibbs, An Environment to Integrate CAD Tools Used in Education, Proceedings, Microelectronic System Education Conference and Exposition, pp. 39-49, San Jose, CA, 1991.
25. A. Dollas, V. Chi, Rapid System Prototyping in Academic Laboratories of the 1990's , Proceedings, First International IEEE Workshop on Rapid System Prototyping RSP-90, pp. 38-45, Computer Society Press, 1991.
26. G. L. Gastrodale, A. Dollas, W.T.Krakow, "An Interactive Environment for the Transparent Logic Simulation and Testing of Integrated Circuits", in Proceedings of the 1990 International Test Conference ITC-90, pp. 394-403, Computer Society Press, 1990.
27. A. Dollas, G. L. Gastrodale, W. T. Krakow, "A. Knowledge - Based Environment for the Integration of Logical and Physical Testing of VLSI Circuits", in Proceedings, First IEEE Workshop on Tools for Artificial Intelligence TAI-89, pp. 259-265, Computer Society Press, 1989.
28. A. Dollas, "What is Next in Real-Time Computer Vision? - An Overview of Nonhomogeneous Multiprocessor Architectures", Proceedings, IEEE Workshop on Languages for Automation LFA-88, pp. 204-211, Computer Society Press, 1988.

**F. Short or Poster Conference Papers, (Refereed)**

1. G. Chrysos, A. Dollas, N.Bourbakis, S. Mertoguno, An Integrated Video Compression, Encryption and Information Hiding Architecture based on the SCAN Algorithm and the STRETCH Technology, *Proceedings of the 15th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2007),* pp. 327-330, Napa Valley, April, 2007.
2. E. Sotiriades, A. Dollas, "Design Space Exploration for the BLAST Algorithm Implementation," *Proceedings of the 15th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2007),* pp. 323-326, Napa Valley, April, 2007.
3. K. Papadimitriou, A. Dollas, A. Anyfantis, Methodology and Experimental Setup for the Determination of System-level Dynamic Reconfiguration Overhead, *Proceedings of the 15th IEEE International Symposium on Field Programmable Custom Computing Machines (FCCM '07),* pp. 335-336, Napa CA, USA, April 2007.
4. K. Papadimitriou, A. Dollas, Performance Evaluation of a Preloading Model in Dynamically Reconfigurable Processors, *IEEE Conference on Field Programmable Logic and Applications (FPL '06)*, pp. 901-904, Madrid, Spain, August 2006.
5. K. Papademetriou, A. Dollas, A Task Graph Approach for Efficient Exploitation of Reconfiguration in Dynamically Reconfigurable Systems, Proceedings, IEEE Symposium on Field Programmable Computing Machines (FCCM), Napa Valley, USA, April 24-26, 2006, Computer Society Press

6. D. Efstathiou, K. Kazakos, A. Dollas, Parrotfish: Task Distribution in an ad hoc Sensor Network through Dynamic Run Time Reconfiguration, Proceedings, IEEE Symposium on Field Programmable Computing Machines (FCCM), Napa Valley, USA, April 24-26, 2006, Computer Society Press.
7. H Sofikitis, K. Roumpou, A. Dollas, N. Bourbakis, "An Architecture for Video Compression Based on the SCAN Algorithm", Proceedings, IEEE Symposium on Field Programmable Computing Machines (FCCM), pp. 295-296, Napa Valley, USA, April, 2005.
8. A. Dollas, I. Ermis, I. Koidis, et al., "An Open TCP/IP Core for Reconfigurable Logic", Proceedings, IEEE Symposium on Field Programmable Computing Machines (FCCM), pp. 297-298, Napa Valley, USA, April, 2005
9. A. Dollas, D. Efstathiou, G Vernardos, et al., "On Distributed Reconfigurable Systems: Open Problems and Some Initial Solutions", Proceedings, IEEE Symposium on Field Programmable Computing Machines (FCCM), pp. 335-336, Napa Valley, USA, April, 2005.
10. S. Sotiropoulos, K. Papademetriou and A. Dollas, "Adaptation of a Low Cost Motion Recognition System for Custom Operation from Shrink-Wrapped Hardware", Proceedings of the Biometrics Methods and Applications Workshop (WBMA Workshop) November 8, 2003, San Diego, USA
11. A. Dollas, K. Papademetriou, S. Sotiropoulos, and E. Sotiriades, A Device to Interface with the Environment for Kinetically Challenged Persons, Proceedings of the 7th Panhellenic Conference on Rehabilitation Medicine, pp. 82-83, Chania, Greece, October 2003.
12. K. Papademetriou, A. Dollas, S. Sotiropoulos, "A Second Generation Embedded Reconfigurable Input Device for Kinetically Challenged Persons", in Proceedings, 11th International IEEE Symposium on Field-Programmable Custom Computing Machines, Napa Valley, April 9-11, 2003.
13. A. Dollas, E. Sotiriades, A. Emmanouelides, L. House, General Purpose vs. Custom FCCM's: a Comparison of Splash 2, Quickturn RPM, and GE1 for Golomb Ruler Derivation, Proceedings, 6th International IEEE Symposium on FPGA's for Custom Computing Machines, pp. 269-270, Napa Valley, April, 1998.
14. D. Overhauser, A. Dollas, The GERM Board for Integrating FPGAs into the Entire Digital Design Curriculum, Designing Microelectronic Systems Using FPGAs, a Special Session of the 1994 Frontiers in Education Conference, San Jose, CA, November 4, 1994 (distributed via Mosaic).
15. A. Dollas, Knowledge -Based Systems at Work: Experience From a Knowledge-Based Integrated Circuit Testing System, Proceedings, 1990 International Computer Software and Applications Conference COMPSAC-90, p. 29, IEEE Computer Society Press, 1990.

**G. Invited Conference Papers (Unrefereed)**

1. A. Dolllas, Rapid System Prototyping of Integrated Microelectronic Systems, Conference on Computer Science and Operations Research Applications in the Greek Armed Forces, General Staff of Greek Armed Forces, November 2-3, 1999 (Proceedings in CD-ROM).

**H. Other Publications and Technical Reports**

1. A. Dollas, K. Papademetriou, C. Mathioudakis, E. Markatos, M. Katevenis, Experimental ATM Network Intrerface Performance Evaluation, Technical Report FORTH-ICS/TR-244, February 1999.
2. G.L. Castrolade, A. Dollas, W.T. Krakow, An Interactive Enviroment for the Transparent Logic Simulation and Testing of Integrated Circuits, Microelectronics Center of North Carolina Technical Report TR90-05, 1990 (reprint of the ITC-90 paper).
3. A. Dollas, R. Krick, Compiler vs. Organization Tradeoffs in the Sustained Performance Architecture, Technical Report DU-EE/CEG-90-01, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1990.

4. A. Dollas, R.F. Krick, The Case for the Sustained Performance Computer Architecture, ACM SIGARCH Computer Architecture News, Vol. 17, No. 6, pp. 129-136, December 1989, ACM Press.
5. A. Dollas, A 3-Chip Set for On-the-fly Image Processing, MCNC Microelectronics Technical Bulletin, Vol. 1, Number 1, September/October 1989, p. 3.
6. A. Dollas, R. Krick, B. Milburn, Verification Through Prototyping of a Sustained Performance Architecture, Technical Report DU-EE/CEG-89-01, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1980.
7. A. Dollas, R. Krick, B. Milburn, An Architecture for Sustained Instruction Throughput, Technical Report DU-EE/CEG-89-02, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1989.
8. A. Dollas, R. Krick, B. Milburn, Performance Study of an Architecture for Sustained Instruction Throughput, Technical Report DU-EE/CEG-89-03, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1989.
9. A. Dollas, R. Krick, B. Milburn, Performance Evaluation of an Architecture with a Bubble-Free Instruction Pipeline, Technical Report DU-EE/CEG-88-01, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1988.
10. A. Dollas, B. Milburn, R. Krick, New Techniques for the Performance Evaluation of Instruction Pipelines, Technical Report DU-EE/CEG-88-02, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1988.
11. A. Dollas, An Architecture for the Optimal Execution of Serial Programs With Run-Time Dependencies, Technical Report DU-EE/CEG-87-02, Computer Engineering Group, Dept. of Electrical Engineering, Duke University, 1987.
12. A. Dollas, Architecture and Applications of a UNIFIELD -Type Computer, University of Illinois at Urbana-Champaign, Department of Computer Science Technical Report UIUCDCS-R-87-1348, June 1987 (Ph.D.Thesis).
13. A. Dollas, Spectrum Sample Transmission: A New Concept in Wavelength Division Multiplexing, University of Illinois at Urbana-Champaign, Department of Computer Science Technical Report UIUCDCS-R-84-1172, May, 1984 (M.S.Thesis).

**PATENTS**

1. A. Dollas, R.F. Krick, B.D. Milburn, Method and Apparatus for Using Extracted Program Flow Information to Prepare for Execution Multiple Instruction Streams, United States Patent No. 5,050,068, September 17, 1991.

**AWARDS AND HONORS**

1996 "IEEE Computer Society Golden Core Member" (Award to roughly 500 of the 100.000 members of the IEEE Computer Society who during its first 50 years greatly contributed to the Society).

1992 Invited participant (one of fifteen) by the National Science Foundation (USA) in the "NSF Workshop on Field Programmable Gate Arrays" to determine NSF policy for the diffusion of the (then) new FPGA technology to USA university-level education.

1992 ΤΒΠ

1991 "IEEE Computer Society Meritorious Service Award" for dedicated and significant service as Publications Chair and as Vice-Program Chair of the TAI '90 and TAI '91 Conferences (TAI=Tools for Arificial Intelligence)

1986 HKN

1986 Best Teaching Assistant of the Year Award, Computer Science Department, University of Illinois at Urbana-Champaign (second time).

1985 Certificate of Recognition and Award as Finalist (one out of seven) University-wide Teaching Excellence Award Competition, University of Illinois at Urbana-Champaign (only non-US Citizen among finalists).

1985 Best Teaching Assistant of the Year Award, Computer Science Department, University of Illinois at Urbana-Champaign.

**PROFESSIONAL SOCIETIES**

- IEEE (και Computer Society) Member since 1984, Senior Member since 1993.
- ACM 1987-1993
- HKN, ΤΒΠ.

**PROFESSIONAL ACTIVITIES**

- Reviewer for archival journals including IEEE Transactions on Computers, IEEE Transactions on VLSI Systems, IEEE Transactions on Communications, IEEE COMPUTER, and conferences including IEEE-FCCM, IEEE-RSP, EDAC-EUROASIC, EURO-DAC, EURO-VHDL.
- General co-Chair of the 15th IEEE International Workshop on Rapid System Prototyping (RSP) 2004, Geneva, Switzerland. European Program Chair of the 12$^{th}$ IEEE International Workshop on Rapid System Prototyping (RSP) 2001, Monterey, California, USA.
- Program Committee Member (1993 - present), 1$^{st}$-13$^{th}$ IEEE Symposium on Field Programmable Custom Computing Machines (FCCM), Napa Valley, USA.
- Program Committee Member (2004 - present, IEEE International Conference on Field-Programmable Technology (FPT).
- Program Committee Member (1990 – present), 1$^{st}$–15$^{th}$ IEEE International Workshop on Rapid System Prototyping (RSP), USA and Europe.
- Technical Program Committee, 18th SBCCI 2005 (SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN) which will be held in Florianopolis - Brasil on September 4-7, 2005..
- Program Committee Member, 2003 ACM Workshop on Biometrics: Methods and Applications, USA.
- Program Committee Member, ENREGLE, 2000 (USA), ERSA 2001 (USA).
- Program Committee Member, 1$^{st}$-4$^{th}$ IEEE International Conference on Tools for Artificial Intelligence, 1989-1992.
- Program Committee member, 10$^{th}$ Panhellenic Conference on Informatics, Volos, Greece, November 11-13, 2005.
- Program Committee Member, 5$^{th}$-8$^{th}$ Hellenic Informatics Society Conference, Greece.

**RESEARCH AND EDUCATION PROJECT SUPPORT**

- GSRT PENED 2003, Apostolos Dollas, PI, Manolis Antonidakis, Spyros Blionas, Co-PI's, "Methodology and Technology for the Development of Multiprocessor Wireless Communication Systems and Reconfigurable Computing Circuits", Total budget: 151,200Euros, (TUC Budget roughly 1/3 of the total budget plus overhead for the entire project). Project awarded in 2005.
- "Structures for Reconfigurable Computing", HRAKLEITOS, GSRT, Apostolos Dollas, PI, 32,229 Euros.

- Information Society (3rd EU Framework of Support to Greece), "Advanced Telematic Services – Tele-education" Προγράμματα Γ' ΚΠΣ Κοινωνίας της Πληροφορίας. «Προηγμένες τηλεματικές υπηρεσίες – Τηλέ-εκπαίδευση» (M.10), 216.102 Euros, Technical University of Crete Campus-Wide PI: A. Dollas, 2001-2003.
- Information Society (3rd EU Framework of Support to Greece), "Information Society Related Upgrade of the Technical University of Crete Infrastructure (M. 7), 154.625 Euros. Technical University of Crete Campus-Wide PI: A. Dollas, 2001-2003.
- Greek Secretariat of Research and Technology (GSRT), Program PENED99, "An Experimental Protocol Boosting Platform for ATM Active Networks", DRS 59.000.000 (~173,000 Euros), PI: A. Dollas (Co-PI's: D. Pnevmatikatos – FORTH, M. Antonidakis – Technological Educational Institute of Crete). The proposal received the highest marks in the Computer Science and Engineering CFP.
- Greek Secretariat of Research and Technology (GSRT), and British Council, Program for Greece-UK Cooperation, "A Reconfigurable Input Device for Kinetically Challenged Persons", Greek Budget: DRS 3.094.000 (9,080 Euros), Scotland Budget: DRS 640.000 καί GBP 2,000 (Σκωτία), PI's: A. Dollas (Greece), T. Kean (Scotland), 1999-2000.
- Xilinx Corporation: Donation of 16 licenses of the Foundation Series CAD Tools and 17 XESS Corp. XS40 development systems for FPGA education (commercial value roughly USD 134,000), 1998.
- 2nd EU Framework of Support to Greece, EPEAEK program, "GUNET-Greek Universities Network, Backbone and Access Services", Country-wide Budget 6,7 billion DRS (~19,7 million Euros), Country-wide PI: L. Merakos (University of Athens). Technical University of Crete Budget: 182,006,000 DRS (~534,000 Euros), PI: M. Paterakis, Co-PI: A. Dollas, 1997 (3 year program).
- 2nd EU Framework of Support to Greece, EPEAEK program, "Technical University of Crete Campus-Wide Computer Network", Budget 357.550.000 DRS (~1,050,000 Euros), PI: A. Dollas, Co-PI: M. Paterakis, (3 years).
- National Science Foundation, A Field Programmable Gate Array Based Laboratory for Digital System Design USD 76,029, (PI: A. Dollas, Co-PI's: P. Marinos, D. Overhauser), 1993.
- National Science Foundation, Research Experiences for Undergraduates Supplement to the project Rapid System Prototyping through Increased Subsystem Reusability, USD 7,750, REU Supplement to Grant Number MIP-9209866, 1992 (3 year grant).
- National Science Foundation, Rapid System Prototyping through Increased Subsystem Reusability, USD 88,314, Grant Number MIP-9209866, 1992 (3 year grant).
- CADRE Technologies, Inc. donation of a six station installation of the full suite of the CASE tool Teamwork, USD 215,000, 1991.
- Westinghouse Foundation, Curriculum Development in Advanced Digital System Design, USD 90,000, 1990 (3 year grant).
- Lord Foundation, Development of Class Notes in Advanced Digital System Design, USD 3,000, 1991.
- National Science Foundation (through University of Hawaii administered program), Development Boards and Software for Field Programmable Gate Arrays, USD 2,000, 1990.
- Hewlett-Packard, grant of five logic analyzers for undergraduate laboratories, $24,685, and a computer workstation used for VLSI testing , USD 42,500, 1988.
- Lord Foundation, Upgrade of the Logic Design Laboratory, USD 5,800, 1988.
- National Science Foundation, Equipment for Systems Prototyping and Verification Laboratory, USD 38,000, (PI: G. Kedem, Co-PI's: J. Board, A. Dollas, J. Ellis), CCR-8716838, 1988.
- North Carolina Board of Science and Technology, Infrastructure Development for New Research Programs in the Department of Electrical Engineering at Duke University, USD 27,500, (Co-PI's: J. Board, A. Dollas) 1988.

- Donation of seven video cameras for the real-time computer vision project at Duke, General Electric, USD 17,500, 1987.
- Duke University, Study of an Architecture for Real-Time Applications with Execution Time Dependencies, Duke University, URC Major Grant, USD 5,000, 1987.

**INVITED LECTURES**

1. "FPGA Based Architecture for DNA Sequence Comparison and Match", Virginia Tech, USA (3/20/2006)
2. "*Configurable Computing Research at MHL – 2001*", Imperial College, London, (9/6/2001).
3. "*Configurable Computing Research at MHL*", ALBA Center and University of Edinburgh – Σκωτία, (3/6/00), also at Xilinx Corp. Edinburgh, Scotland, (3/10/00), Computer Science Department, University of California at San Diego (4/19/00).
4. "*A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition using Hidden Markov Models*", ALBA Center and University of Edinburgh – Scotland, (3/6/00).
5. *New Applications of Computer Technology in the Armed Forces, V Division of the Greek Army, Chania, Greece (4/28/99)*
6. *Defense Applications of Recent Developments in Computer Technology, V Division of the Greek Army, Chania, Greece (10/25/95)*
7. *Current Research Issues in Rapid Microelectronics System Prototyping and Relevant Recent Results from the Duke University*, invited distinguished lecturer at the University of Louisville, Kentucky (8/10/92).
8. *Knowledge Based Concurrent Scheduling of Multi-Process Applications on Symmetric Microprocessors*, invited lecture at the Department of Electrical Engineering and Department of Computer Science, SUNY Binghamton (7/20/92).
9. *Experience and Future Directions in the use of Field Programmable Gate Arrays in the Electrical Engineering Program at Duke University*, National Science Foundation Workshop on Field Programmable Gate Arrays ,July 16-17,1992, Washington DC, (7/16/92).
10. *A Sustained Performance Architecture*, MasPar Computer Corporation, Sunnyvale, California (11/12/91).
11. *Experimental Results in Rapid System Prototyping with Incomplete CAD Tools and Inexperienced Designers*, University of Patras, Greece (7/10/91), also, Department of Computer Science, University of North Carolina at Chapel Hill (1/29/92).
12. *Program Flow Graph Aided Sustained Instruction Prefetching from Slow Main Memory to Fast Processors*, University of Crete, Greece (6/25/91).
13. *Computer Architecture: Current Problems in Computer Design and Some Possible Solutions*, North Carolina Supercomputing Center (2/20/91).
14. *Compiler Issues for Instruction Perfecting in the Sustained Performance Architecture*, Center for Supercomputing Research and Development, University of Illinois at Urbana-Champaign (7/3/90).
15. *A Knowledge-Based Environment for the Integration of Logical and Physical Testing of VLSI Circuits*, Open Architecture Silicon Implementation System Group(OASIS),MCNC Tele-seminar (11/89).
16. *The Application of Hewlett-Packard Logic Analyzers in the Electrical Engineering Curriculum at Duke University*, Hewlett-Packard University Affiliates Conference (6/20/89).
17. *An Architecture for Sustained Performance Computing*, lecture and computer demonstration at Duke University (4/26/89); also lectures at the University of Crete, Greece (5/17/89), and North Carolina State University (7/11/89).
18. *Non-Homogenous Multiprocessors for Real-Time Computer Vision*, University of Crete (7/11/89).

19. *Real-Time Image Processing Systems Efforts at Duke*, mini-conference on "Robotics Related Research at the Duke School of Engineering", Duke University (3/20/89).
20. *On Chaotic Computing*, Computer Engineering Colloquium, Dept. of Electrical Engineering, Duke University (10/21/87).

**PH.D. DISSERTATION SUPERVISION**

1. **J. D. S. Babcock**, Synthesis of Microelectronic Systems with Reusability of Nonsynthesizable Subsystems, Duke University, Department of Electrical Engineering, 1995.
2. **Keith V. Boland**, An Evaluation of the Uses of Program Control Flow Information in Instruction Memory Hierarchies: Prefetching and Predictability, Duke University, Department of Electrical Engineering, 1993.
3. **Robert F. Krick**, An Instruction Memory Organization for High Performance Instruction Sequencing, Duke University, Department of Electrical Engineering, 1991.

**MS THESES SUPERVISION**

1. **William T. Rankin**, Optimal Golomb Rulers: An Exhaustive Parallel Search Implementation, Duke University, Department of Electrical Engineering, 1993.
2. **Jeffrey B. Messinger**, A Study of Program Flow Graphs and their Application to the Sustained Performance Architecture, Duke University, Department of Electrical Engineering, 1993.
3. **Brent Ward**, An Experimental Study in Subsystem Reusability Toward Rapid Prototyping of Microelectronic Systems, Duke University, Department of Electrical Engineering, 1993.
4. **Lee House**, Programming FPGA Based Custom Computing Engines in VHDL to Solve Computationally Intensive Problems, Duke University, Department of Electrical Engineering, 1993.
5. **Scott Witscher**, A Quantitative Analysis of the Sustained Performance Architecture, Duke University, Department of Electrical Engineering, 1992.
6. **J. D. Sterling Babcock**, An Experimental Study in Microelectronic System Design, Duke University, Department of Electrical Engineering, 1992.
7. **William D. Elliott**, Design and Performance Evaluation of a Real-Time Image Processing Chip for Computer Vision, Duke University, Department of Electrical Engineering, 1992.
8. **Kunihiko Nakada**, A Detailed Simulation of the Sustained Performance Architecture for the MIPS Microprocessor, Duke University, Department of Electrical Engineering, 1992.
9. **Philip J. Christopher**, Knowledge Based Process Scheduling of Multi-Task Applications on Symmetric Multiprocessors, Duke University, Department of Electrical Engineering, 1991.
10. **Grant L. Castrodale**, An Integrated Environment for the Simulation and Testing of VLSI Circuits, Duke University, Department of Electrical Engineering, 1989.
11. **James Dodrill**, ARIEL: A Writeable Control Store Computer Architecture Supporting Transparent Vertical Migration, Duke University, Department of Electrical Engineering, 1989.
12. **Robert F. Krick**, An Architecture with Bubble-Free Instruction Pipeline Operation, Duke University, Department of Electrical Engineering, 1989.
13. **Dimitris Pantzartzis**, Design and VLSI Implementation of a Real-Time Image Processing Chip Set, Duke University, Department of Electrical Engineering, 1989.
14. **Blair D. Milburn**, Instruction Decoding for a Sustained Performance Architecture, Duke University, Department of Electrical Engineering, 1988.